Homework
Part 1: Virtualization – 4) Memory 2

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1 Page Numbers and Offsets

1.1 16-bit Virtual Address Space / 8-bit VPN

Assuming a 16-bit virtual address space and a virtual page number (VPN) of 8 bits.

1. How many bits is the offset? How many addresses does a single page contain (i.e. what is the page size)?
2. For each of the following addresses, compute the VPN and the offset within the page:
   - `0x01cd`
   - `0x34ff`
   - `0xff5c`
   - `0x01a0`
   - `0x5689`

1.2 16-bit Virtual Address Space / 6-bit VPN

Assuming a 16-bit virtual address space and a virtual page number (VPN) of 6 bits.

1. How many bits is the offset? How many addresses does a single page contain (i.e. what is the page size)?
2. For each of the following addresses, compute the VPN and the offset within the page:
   - `0x01cd`
   - `0x34ff`

- `0xff5c`
- `0x01a0`
- `0x5689`

1.3 32-bit Virtual Address Space (Multi-Level Page Table)

Assuming a 32-bit virtual address space, an 8-bit page directory index (PDI) and a 12-bit page table index (PTI).

1. How many bits is the virtual page number (VPN)?
2. How many bits is the offset? How many addresses does a single page contain (i.e. what is the page size)?
3. For each of the following addresses, compute PDI, PTI and offset:
   - `0x01cd34ff`
   - `0xff5c01a0`
   - `0x568990aa`
   - `0x01000104`

2 Page Table Size

2.1 16-bit Virtual Address Space

Assuming a 16-bit virtual address space and a page size of 512 bytes.

1. How many bits are required for the offset?
2. Suppose each page table entry (PTE) has a size of 4 bytes. How large is the entire page table?

2.2 48-bit Virtual Address Space

Assuming a 48-bit virtual address space and a page size of 4096 bytes, with page table entries (PTE) requiring 4 bytes each.

1. How large is the page table for a single process?
2. How much memory is required for managing pages when there are 100 processes running?

2.3 48-bit Virtual Address Space With Multi-Level Page Table

As we can see in 2.2, managing memory with linear page tables is not feasible for this address space. Instead, a multi-level page table shall be used:

- As indicated, page table entries (PTE) are 4 bytes each.
- Each chunk of the page table must fit in a single page (4096 bytes).

How many levels are required for the page table?

3 Accessing Memory With a TLB

The objective of the translation look aside buffer (TLB) is to reduce memory access time by taking advantage of the locality of reference principle.

Assuming that accessing the main memory (RAM) takes 80 ns and the time required for accessing the TLB is 5 ns, *what is the minimal TLB hit rate* such that the average memory access time is at most 35 ns?

👉 The average memory access time is the sum of the average time of both accesses, with and without TLB.

4 Linux Huge Pages ★

Read [lwna] and [lwnb] to find out more about the support for huge pages in the Linux Kernel and its impact on performance.

References

[lwna] *lwn.net, Huge pages part 1 (Introduction)*, https://lwn.net/Articles/374424/.

[lwnb] *lwn.net, Huge pages part 4: benchmarking with huge pages*, https://lwn.net/Articles/378641/.